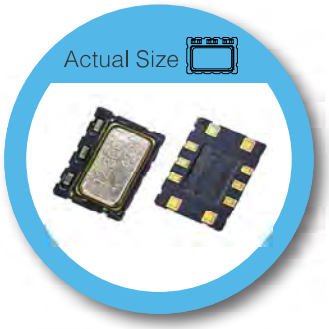
TAITIEN
Our Performance, Your Reputation

TS Type < for Stratum 3 >

7.0 x 5.0 mm SMD Stratum 3 Voltage Controlled Temperature Compensated Crystal Oscillator



RoHS Compliant

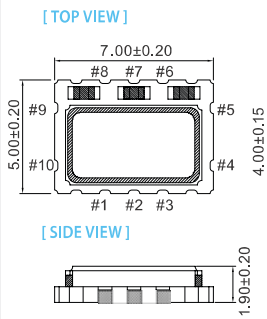
FEATURE

- Typical 7.0 x 5.0 x 1.9 mm ceramic SMD package.
- Stratum 3 (Overall ±4.6ppm including 20 years aging.)
- CMOS and Clipped Sine wave (without DC-cut capacitor) output optional.

TYPICAL APPLICATION

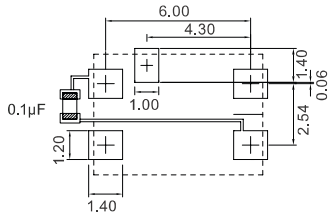
- Base Stations
- Stratum 3

DIMENSION (mm)



Pin#	Function
1	NC
2	NC
3	NC
4	GND
5	Output
6	NC
7	NC
8	Tri-State/NC
9	VDD
10	Vcon:VC-TCXO GND/NC:TCXO

SOLDER PAD LAYOUT (mm)



To ensure optimal oscillator performance, place a by-pass capacitor of 0.1μF as close to the part as possible between Vdd and GND pads.

ELECTRICAL SPECIFICATION

Parameter		5.0 V		3.3V		Unit
		Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		5	52	5	52	MHz
Standard Frequency (for CMOS)		8.192, 10, 12.8, 20				
Standard Frequency (for Clipped sine Wave)		8.192, 10, 12.8, 16.384, 19.2, 19.44, 20, 25, 26				
Operating Temp. Range		-20 ~ 70 -40 ~ 85				°C
Frequency Stability (Overall, 20 Years)*		–	±4.6	–	±4.6	ppm
Frequency Stability Vs Temp. Range		–	±0.28	–	±0.28	ppm
Holdover Stability +		–	±0.37	–	±0.37	ppm
Supply Current (CMOS output)		–	6.0	–	6.0	mA
Supply Current (Clipped Sine Wave)		–	3.5	–	3.5	
Output Level (CMOS)						
Output High (Logic"1")		90%VDD	–	90%VDD	–	V
Output Low (Logic"0")		–	10%VDD	–	10%VDD	
Duty		45	55	45	55	%
Output Level (Clipped Sine Wave)		0.8	–	0.8	–	Vp-p
Load (CMOS)		15pF		15pF		
Load (Clipped Sine Wave)		10 KΩ // 10pF		10 KΩ // 10pF		
Control Voltage Range (VCTCXO)		0.5	2.5	0.5	2.5	V
Pulling Range (VCTCXO)		±5.0	–	±5.0	–	ppm
Vc Input Impedance (VCTCXO)		100	–	100	–	kΩ
Phase Noise @ 10 MHz	100 Hz	-120		-120		dBc / Hz
	1 kHz	-140		-140		
	10 kHz	-148		-148		
Start Time		–	2	–	2	mSec
Tri-State						
Disable		–	1.5	–	0.99	V
Enable		3.5	–	2.31	–	
Storage Temp. Range		-55	125	-55	125	°C

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
* Including calibration @ 25°C, supply voltage VDD±5% , load 15pF±5%, reflow soldering, 20 years aging and frequency stability over temperature.
+ Including 24hours aging , supply voltage VDD±5% and frequency stability over temperature.

Note: not all combination of options are available. Other specifications may be available upon request.