

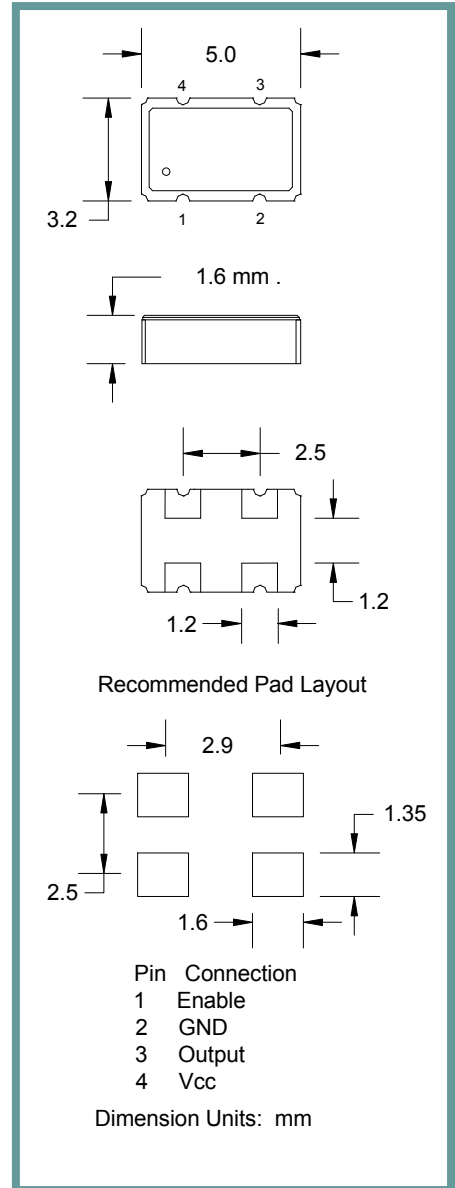
**Product Features:**

Low Jitter, Non-PLL Based Output  
 CMOS/TTL Compatible Logic Levels  
 Compatible with Leadfree Processing

**Applications:**

Fibre Channel  
 Server & Storage  
 Sonet /SDH  
 802.11 / Wifi  
 T1/E1, T3/E3  
 System Clock

<b>Frequency</b>	1.5 MHz to 125.000 MHz
<b>Output Level</b> HC-MOS TTL	'0' = 0.1 Vcc Max., '1' = 0.9 Vcc Min. '0' = 0.4 VDC Max., '1' = 2.4 VDC Min.
<b>Duty Cycle</b>	Specify 50% ±10% or ±5% See Table in Part Number Guide
<b>Rise / Fall Time</b>	5 nS Max. @ Vcc = +3.3 VDC, 10 nS Max. @ Vcc = +5 VDC ***
<b>Output Load</b>	Fo < 50 MHz = 10 TTL, Fo > 50 MHz = 5 LSTTL See Table in Part Number Guide
<b>Frequency Stability</b>	See Frequency Stability Table (Includes room temperature tolerance and stability over operating temperature)
<b>Start-up Time</b>	10 mS Max.
<b>Enable / Disable Time</b>	100 nS Max. N.C. or ≥ 70% Vdd = Enable. ≤ 30% Vdd = Disable.
<b>Supply Voltage</b>	See Input Voltage Table, tolerance ±5 %
<b>Current</b>	40 mA Max. ***
<b>Operating</b>	See Operating Temperature Table in Part Number Guide
<b>Storage</b>	-55° C to +125° C
<b>Jitter: RMS(1sigma)</b> 1 MHz-75 MHz 76 MHz-80 MHz	5 pS RMS (1 sigma) Max. accumulated jitter (20K adjacent periods) 3 pS RMS (1 sigma) Max. accumulated jitter (20K adjacent periods)
<b>Max Integrated</b> 1 MHz-75 MHz 76 MHz-80 MHz	1.5 pS RMS (1 sigma -12KHz to 20MHz) 1 pS RMS (1 sigma -12KHz to 20MHz)
<b>Max Total Jitter</b> 1 MHz-75 MHz 76 MHz-80 MHz	50 pS p-p (100K adjacent periods) 30 pS p-p (100K adjacent periods)



Part Number Guide		Sample Part Number:		ISM92 - 3251BH - 20.000			
Package	Input Voltage	Operating Temperature	Symmetry (Duty Cycle)	Output	Stability (in ppm)	Enable / Disable	Frequency
ISM92 -	5 = 5.0 V	1 = 0° C to +70° C	5 = 45 / 55 Max.	1 = 10TTL / 15 pF HC-MOS	**E = ±10	H = Enable	- 20.000 MHz
	3 = 3.3 V	6 = -10° C to +70° C	6 = 40 / 60 Max.	6 = 30 pF	**D = ±15	O = N/C	
	7 = 3.0 V	3 = -20° C to +70° C		5 = 50 pF HC-MOS (<40 MHz)	**F = ±20		
	2 = 2.7 V	4 = -30° C to +75° C			**A = ±25		
	6 = 2.5 V	2 = -40° C to +85° C			B = ±50		
	1 = 1.8 V*				C = ±100		

NOTE: A 0.01 µF bypass capacitor is recommended between Vcc (pin 4) and GND (pin 2) to minimize power supply noise.  
 \* Not available at all frequencies. \*\* Not available for all temperature ranges. \*\*\* Frequency, supply, and load related parameters.



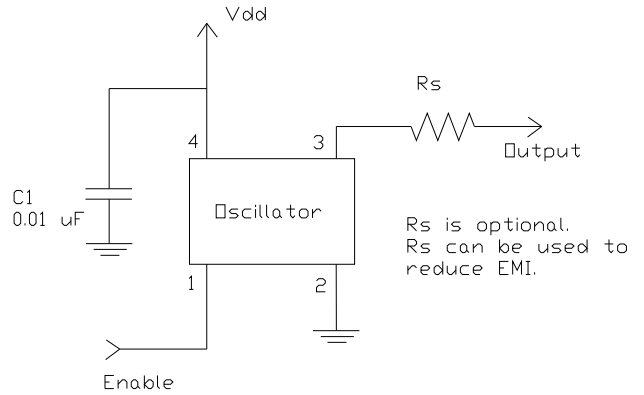
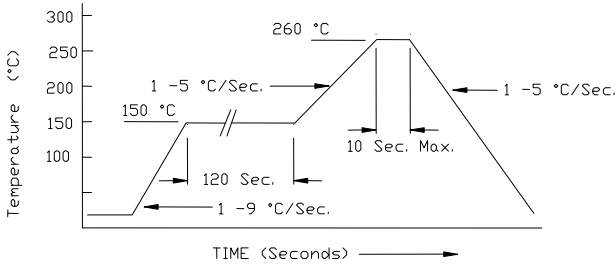
3.2 mm x 5 mm Ceramic Package SMD Oscillator, TTL / HC-MOS



ISM92 Series

**Pb Free Solder Reflow Profile:**

**Typical Application:**

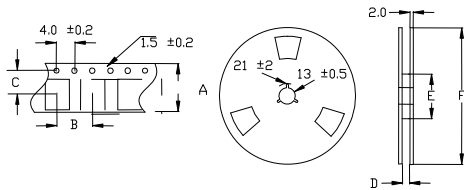


\*Units are backward compatible with 240C reflow processes

**Package Information:**

MSL = N.A. (package does not contain plastic, storage life is unlimited under normal room conditions).  
Termination = e4 (Au over Ni over W base metalization).

**Tape and Reel Information:**



Quantity per Reel	1000
A	16 +/- .3
B	8 +/- .2
C	7.5 +/- .2
D	17.5 +/- .1
E	50 / 60 / 80
F	180 / 250

**Environmental Specifications**

Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Mechanical Vibration	MIL-STD-883, Method 2007, Condition A
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free devices (except 2 cycles max)
Hazardous Substance	Pb-Free / RoHS / Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1=2x10-8 atm cc/s
Solvent Resistance	MIL-STD-202, Method 215

**Marking**

Line 1: ILSI and Date Code (YWW)  
Line 2: Frequency