5x7mm Precision TCXO Model DV75C

Description:

The Connor-Winfield's DV75C is a 5x7mm Surface Mount Temperature Compensated Crystal Controlled Oscillator (TCXO) with LVCMOS output. Through the use of Analog Temperature Compensation the DV75C is capable of holding sub 1-ppm stabilities over the -40 to 85°C temperature range. The DV75C meets STRATUM 3 requirements.

Features:

- 3.3 Vdc Operation
- LVCMOS Output
- Frequency Stability: ± 0.28 ppm
- Temperature Range: -40 to 85°C
- Low Jitter <1ps RMS
- 5x7mm Surface Mount Package
- Tape and Reel Packaging
- RoHS Compliant / Pb Free

Applications:

- IEEE 1588 Applications
- Synchronous Ethernet slave clocks, ITU-T G.8262 EEC options 1 & 2
- Compliant to Stratum 3, GR-1244-CORE, GR-253-CORE & ITU-T-G.812 Type IV
- Wireless Communications
- Small Cells
- Test and Measurement

Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	85	°C	
Supply Voltage (Vcc)	-0.5	-	6.0	Vdc	
Input Voltage	-0.5	-	Vcc+0.5	Vdc	

Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Nominal Frequencies (Fo) available		10.0, 12.8, 20.0, 25.0 and 40.0		MHz	
Frequency Calibration @ 25 °C	-1.0	-	1.0	ppm	1
Frequency Stability vs. Temperature	-0.28	-	0.28	ppm	2
Holdover Stability (Over 24 Hours)	-0.32	-	0.32	ppm	3
Frequency vs. Load Stability	-0.05	-	0.05	ppm	±5%
Frequency vs. Voltage Stability	-0.05	-	0.05	ppm	±5%
Static Temperature Hysteresis	-	-	0.4	ppm	4
Total Frequency Tolerance:	-4.6	-	4.6	ppm	5
Operating Temperature Range:	-40	-	85	°C	
Supply Voltage (Vcc)	3.135	3.3	3.465	Vdc	±5%
Supply Current (Icc)	-	-	6	mA	
Period Jitter	-	3	5	ps rms	
Integrated Phase Jitter	-	0.5	1.0	ps rms	6
Typical Phase Noise Fo = 10.0 MHz					
SSB Phase Noise at 10Hz offset	-	-99	-	dBc/Hz	
SSB Phase Noise at 100Hz offset	-	-122	-	dBc/Hz	
SSB Phase Noise at 1KHz offset	-	-145	-	dBc/Hz	
SSB Phase Noise at 10KHz offset	-	-152	-	dBc/Hz	
SSB Phase Noise at 100KHz offset	-	-153	-	dBc/Hz	
Start-up Time	-	-	10	ms	

LVCMOS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	15	-	pF	7
Voltage (High) (Voh)	90%Vcc	-	-	Vdc	
(Low) (Vol)	-	-	10%Vcc	Vdc	
Duty Cycle at 50% of Vcc	45	50	55	%	
Rise / Fall Time 10% to 90%	-	-	8	ns	

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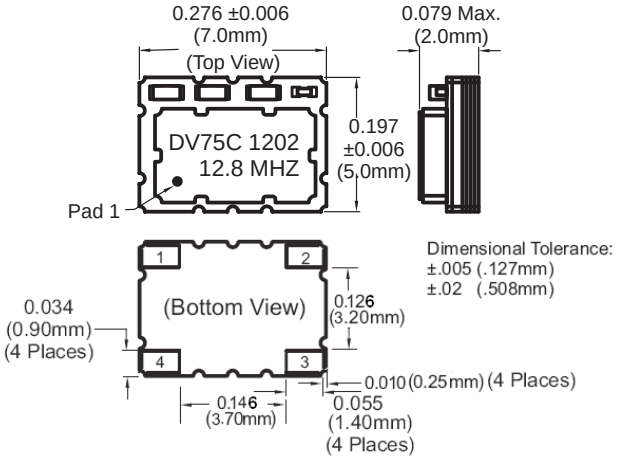
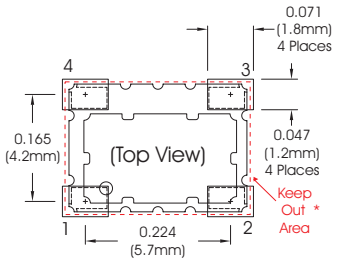
Package Layout

Applies to all frequencies except for 40.0MHz



Suggested Pad Layout



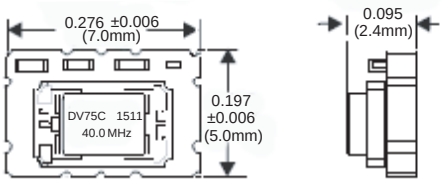
** Do not route any traces in the keep out area. It is recommended the next layer under the keep out area is to be ground plane.*

Pad Connections

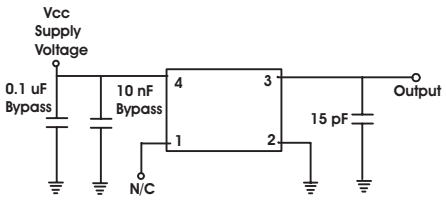
1:	N/C
2:	Ground
3:	Output (Fo)
4:	Supply Voltage (Vcc)

Alternate Package Layout

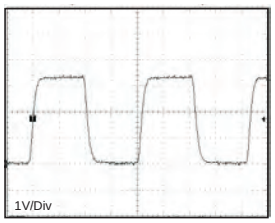
Applies to 40.0MHz frequency only.



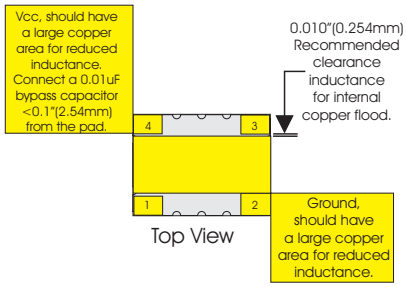
Test Circuit

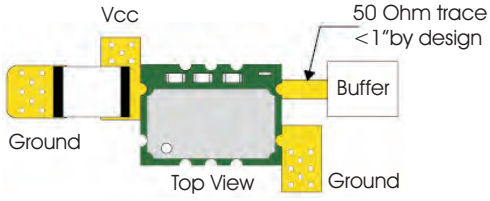


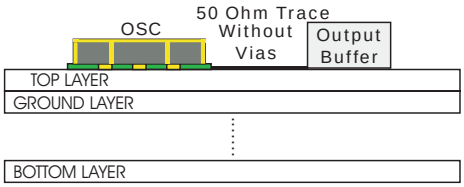
Output Waveform



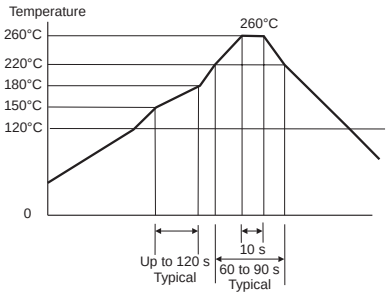
Design Recommendations







Solder Profile



Meets IPC/JEDEC J-STD-020C