

February 2016



- Pletronics' LV77D Series is a quartz crystal controlled precision square wave generator with an LVDS output.
- The package is designed for high density surface mount designs.
- Low cost mass produced oscillator.
- Tape and Reel or cut tape packaging is available.
- 5 x 7 mm LCC Ceramic Package
- Enable/Disable Function on pad 1
- Disable function includes low standby power mode
- Low Jitter
- 80 MHz ~ 325 MHz

Pletronics Inc. certifies this device is in accordance with the RoHS 6/6 (2011/65/EC) and WEEE (2002/96/EC) directives.

Pletronics Inc. guarantees the device does not contain the following: Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's

Weight of the Device: 0.16 grams

Moisture Sensitivity Level: 1 As defined in J-STD-020D.1

Second Level Interconnect code: e4

Absolute Maximum Ratings:

Parameter	Unit
V _{CC} Supply Voltage	-0.5V to +5.0V
Vi Input Voltage	-0.5V to V _{CC} + 0.5V
Vo Output Voltage	-0.5V to V _{CC} + 0.5V

Thermal Characteristics

The maximum die or junction temperature is 155°C

The thermal resistance junction to board is 30 to 50°C/Watt depending on the solder pads, ground plane and construction of the PCB.



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Part Number:

· a.c.		~ •	•					
LV77	45	D	E	W	-125.0M	-XX		Part Marking:
							Packaging code or blank T250 = 250 per Tape and Reel T500 = 500 per Tape and Reel T1K = 1000 per Tape and Reel	PLE LV77 FF.FFF M • YMDXX
							Frequency in MHz	LV7XYWWXX
							Supply Voltage V _{cc} W = 2.5V ± 10%	FF.FFF M • PLE XXX
							Optional Enhanced OTR Blank = Temp. range -10 to +70°C C = Temp. range -20 to +70°C E = Temp. range -40 to +85°C	
							Series Model	
							Frequency Stability 45 = ± 50 ppm 44 = ± 25 ppm 20 = ± 20 ppm	
							Series Model	

Marking Legend:

PLE = Pletronics

FF.FFF M = Frequency in MHz

YYWW or YWW or YMD = Date of Manufacture (year and week, or year-month-day)

All other marking is internal factory codes

Specifications such as frequency stability, supply voltage and operating temperature range, etc. are not identified from the marking. External packaging labels and packing list will correctly identify the ordered Pletronics part number.

Codes for Date Code YMD

Code	4	5	6	7	8	Code	A	В	C	D	E	F	G	Н	J	K	L	M
Year	2014	2015	2016	2017	2018	Month	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
C	Code		1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F	G
	Day		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
C	Code		Н	J	K	L	М	N	Р	R	Т	U	٧	W	Х	Υ	Z	
	Day		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
				•								•		•				



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Electrical Specification for 2.50V $\pm 10\%$ over the specified temperature range and the frequency range of 80 to 325 MHz

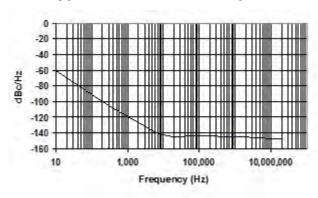
Item	Min	Max	Unit	Condition			
Frequency Accuracy "45"	-50	+50	ppm		voltages, load changes, aging for 1		
"44"	-25	+25		year, shock, vibration and temperatures			
" 20 "	-20	+20					
Output Waveform		LVDS					
Output High Level		1.60	Volts	See load circu	iit R1 = 50 ohms		
Output Low Level	0.90		Volts				
Differential Output (V _{OD})	250	450	mVolts				
Differential Output Error (dVos)		50	mVolts				
Output Offset Voltage (Vos)	1.125	1.375	Volts	<u>></u> 80 MHz	See load circuit R1 = 50 ohms		
	1.125	1.500	Volts	< 80 MHz			
Output Symmetry	45	55	%	Referenced to	50% of amplitude or crossing point		
Output T _{RISE} and T _{FALL}	300	700	pS	Vth is 20% an	d 80% of waveform ≥ 80 MHz		
	400	900	pS	Vth is 20% an	d 80% of waveform < 80 MHz		
Jitter	-	0.6	pS RMS	Measured from	n 12KHz to 20MHz from Fnominal		
	-	2.8		Measured from	n 10Hz to 1MHz from Fnominal		
Vcc Supply Current	-	63	mA	≥ 80 MHz	Includes current of properly		
	-	40	mA	< 80 MHz	terminated device		
Enable/Disable Internal Pull-up	50	-	Kohm	To Vcc (equiva	alent resistance)		
V disable	•	0.4	Volts	Referenced to	Ground		
V enable	2.0	-	Volts				
Output leakage $V_{OUT} = V_{CC}$	-10	+10	uA	Pad 1 low, dev	vice disabled		
$V_{OUT} = 0V$	-10	+10	uA				
Enable time	-	2	m	Time for outpu	ut to reach a logic state		
Disable time	-	200	nS	Time for outpu	ut to reach a high Z state		
Start up time	-	5	mS	≥ 80 MHz	Measured from the time		
	-	3	mS	< 80 MHz	Vcc = 2.2V		
Operating Temperature Range	-10	+70	°C	Standard Temperature Range			
	-20	+70	°C	Extended Temperature Range "C" Option Extended Temperature Range "E" Option			
	-40	+85	°C				
Storage Temperature Range	-55	+125	°C				
Standby Current I _{cc}	-	3	uA	Pad 1 low, dev	vice disabled ≥ 80 MHz		
	-	1.5	mA	Pad 1 low, device disabled < 80 MHz			

Specifications with Pad 1 E/D open circuit

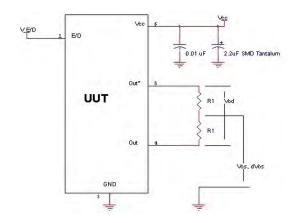


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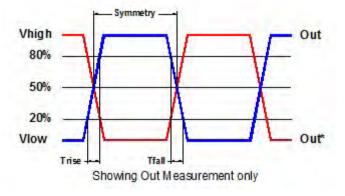
Typical Phase-Noise Response



Load Circuit



Test Waveform





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Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002, Condition B
Vibration	MIL-STD-883 Method 2007, Condition A
Solderability	MIL-STD-883 Method 2003
Thermal Shock	MIL-STD-883 Method 1011, Condition A

ESD Rating

Model	Minimum Voltage	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

Package Labeling

Label is 1" x 2.6" (25.4mm x 66.7mm) Font is Courier New Bar code is 39-Full ASCII Label is 1" x 2.6" (25.4mm x 66.7mm) Font is Arial

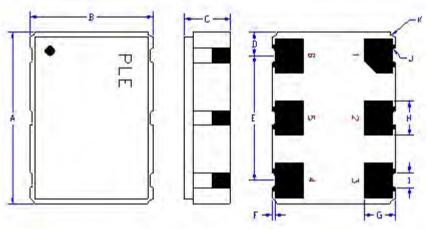
 RoHS Compliant 2nd LvL Interconnect Category=e4

Max Safe Temp=260C for 10s 2X Max



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Mechanical:



	Inches	mm
Α	0.276 <u>+</u> 0.006	7.00 <u>+</u> 0.15
В	0.197 <u>+</u> 0.006	5.00 <u>+</u> 0.15
С	0.067 max	1.70 max
D¹	0.038	0.96
E¹	0.200	5.08
F¹	0.004	0.10
G¹	0.050	1.27
H¹	0.055	1.40
l ¹	0.024	0.60
J ¹	0.004R	0.10R
K¹	0.008R	0.20R

Contacts (pads):

Gold 11.8 to 39.4μinches (0.3 to 1.0μm) over

Nickel 50 to 350µinches (1.27 to 8.89µm)

¹ Typical dimensions

Not to Scale

Pad	Function	Note
1	Output Enable/Disable	When this pad is not connected the oscillator shall operate. When this pad is <0.30 volts, the output will be inhibited (high impedance state.) Recommend connecting this pad to $V_{\rm cc}$ if the oscillator is to be always on.
2	No connect	There is no internal connection to this pad
3	Ground (GND)	
4	Output	The outputs must be terminated, 100 ohms between the outputs is the ideal
5	Output*	termination.
6	Supply Voltage (V _{cc})	Recommend connecting appropriate power supply bypass capacitors as close as possible.

Lead free

Layout and application information

Recommend connecting Pad 1 and Pad 2 together to permit the design to accept Enable/Disable on both input pads

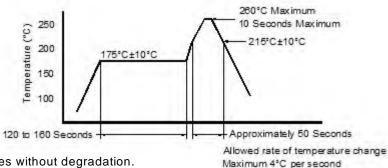
For Optimum Jitter Performance, Pletronics recommends:

- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply
- do not place near piezoelectric buzzers or mechanical fans.



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Reflow Cycle (typical for lead free processing)



The part may be reflowed 3 times without degradation.

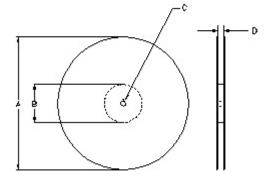
Tape and Reel: available for quantities of 250 to 1000 per reel, cut tape for < 250

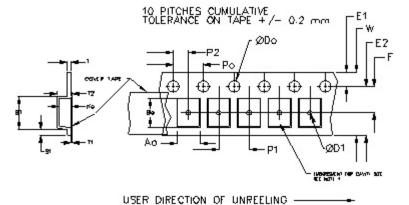
	Constant Dimensions Table 1										
Tape Size	D0	D1 Min	E1	P0	P2	S1 Min	T Max	T1 Max			
8mm		1.0			2.0						
12mm	1.5	1.5	1.75	4.0	<u>+</u> 0.05						
16mm	+0.1 -0.0	1.5	<u>+</u> 0.1	<u>+</u> 0.1	2.0	0.6	0.6	0.1			
24mm		1.5			<u>+</u> 0.1						

	Variable Dimensions Table 2										
Tape Size	B1 Max	E2 Min	F	P1	T2 Max	W Max	Ao, Bo & Ko				
16 mm	12.1	14.25	7.5 <u>+</u> 0.1	8.0 <u>+</u> 0.1	8.0	16.3	Note 1				

Note 1: Embossed cavity to conform to EIA-481-B

Dimensions in mm Not to scale





		REE			
Α	inches	7.0	7.0 10.0		
	mm	177.8	254.0	330.2	
В	inches	2.50	4.00	3.75	
	mm	63.5	101.6	95.3	Tape Width
С	mm	13	vviatri		
D	mm	16.4 +2.0 -0.0	16.4 +2.0 -0.0	16.4 +2.0 -0.0	16.0

Reel dimensions may vary from the above