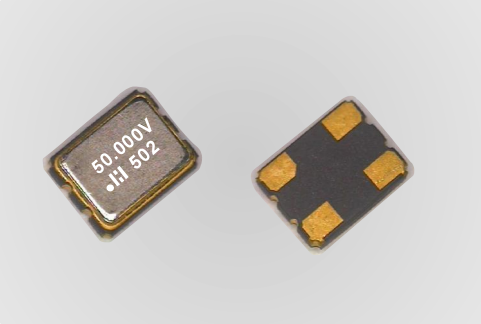
# • D3SV Series 3.2*2.5 VCXO



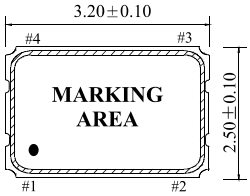

**FEATURES**

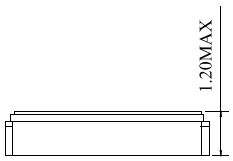
- Industry Standard with 3.2*2.5*1.2mm package
- TTL/HCMOS output compatible
- Tri-State Enable/Disable
- Tight tolerance performance with voltage IC control
- Designed primarily for use in phase lockded loops, phase shift keying and other telecommunication applications such as ADSL, set-top box, and base stations etc.

## Electrical Specifications

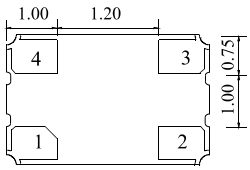
| Parameter | | Condition | D3SV | |
|---|---|---|---|---|
| Frequency Range* | F0 | | 1.75~54MHz | |
| Frequency Calibration | | At 25℃ | ±15ppm | |
| Temperature Stability | | Over $T_{OPR}$ | ±15ppm, ±25ppm, ±50ppm | |
| Stability vs. power change | | $V_{DD}$+/-5% | ±5ppm | |
| Stability vs. load change | | 15pF+/-10% | ±3ppm | |
| Pullability | | Over Control Voltage Range | ±100ppm, ±200ppm | ±100ppm, ±200ppm |
| Control Voltage Range | | | 0.5~4.5V | 0~3.3V |
| Operating Temperature Range | $T_{OPR}$ | | 0℃~+70℃(-40℃~+85℃ option) | |
| Storage Temperature Range | $T_{STG}$ | | -55℃~+125℃ | |
| Power Supply Voltage | $V_{DD}$ | | 5.0V+/-5% | 3.3V+/-5% |
| Aging (First Year) | | 25℃±3℃ | ±5ppm | |
| Supply Current | $I_{DD}$ | | 30mA Max | |
| Output Symmetry | Sym | At 1/2$V_{DD}$ | 40/60%(45/55% Option) | |
| Rise time | $T_r$ | 20%$V_{DD}$~80%$V_{DD}$ | 8nS Max | 10nS Max |
| Fall Time | $T_f$ | 80%$V_{DD}$~20%$V_{DD}$ | 8nS Max | 10nS Max |
| Output Voltage | $V_{OH}$ | | 90% $V_{DD}$ min | |
| | $V_{OL}$ | | 10% $V_{DD}$ max | |
| Output Load | | | 15pF Max | |
| Start-up Time | | Ts | 10mS Max | |
| Packing Unit | | 1000pcs/reel | | |

## Mechanical Dimensions(mm)

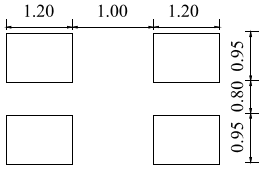


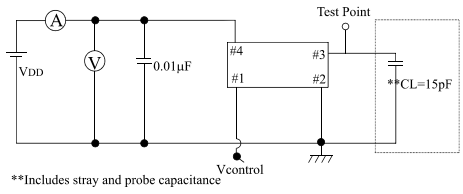

Top View




Recommended Solder Pattern

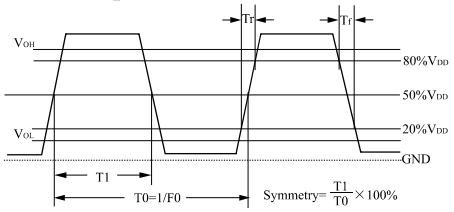



Test Circuit




**Includes stray and probe capacitance

Output Waveform




***note: A 0.01uF bypass capacitor should be placed between $V_{DD}$(Pin6) and GND(Pin3) to Minimize power supply line noise